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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,145	11/17/2003	Cheryl Senter Brashears	SP036.C10	9444

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,145	BRASHEARS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-140* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *136-140* is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☒ Claim(s) *27-29, 34-38,43-45, 80-82, 96-98, 108-110, 48, 54, 62, 72, 87, 94 , 113, 50, 55, 65, 74, 88, 95, 115, 52 57, 60, 67, 76, 77, 90, 91, 104, 105, 117-118 , 49, 65,66, 73, 114,129* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

DANIEL H. PAN
PRIMARY EXAMINER
GROUP 2183

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03,01/22/04,05/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims rejected are 23-26,30-33, 39 , 40-42, 46, 47, 51-53, 56-61, 66-71, 75-79,83-86 89-93,99-103,104-107, 111, 112, 116-119, 120- 128,130-132,133-135 .

1. Claims 23-140 are presented for examination. Claims 1-22 have been canceled.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 23, 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 5,987,593. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the current claim does not recite the load request was made before all instructions as specifically recited in the patent claim 18, one of ordinary skill in the art should be able to recognize the all instructions in the instruction buffer as recited in the patented claim 18 could be applicable for a load before any instructions including a memory request operation, such as a store or a load, in order to enhance the adaptability of the system, therefore, all instructions in system should have included any memory request in the same system. Therefore, for the above reasons given above, it would have been obvious to one of ordinary skill in the art to make the load before a memory request as claimed .

3. As to the "super scalar microprocessor" recited in the current claims23,26, the patented claim 18 already recited "microprocessor" (see preamble) used for executing "plurality of instructions" "out of order" (col.21, lines 1-9, claim 18) , which would have been recognized by one of ordinary skill in the art that execution of plurality of instructions out of order was a characteristic feature of a super scale instructing processing.

4. Claim 33 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 64 of U.S. Patent No. 5,987,593. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the current claim does not recite the load request was made before all instructions as specifically recited in the patent claim 64, one of ordinary skill in the art should be able to recognize that the all instructions in the instruction window as recited in the patented claim 33 could be applicable for a load before any instructions including a memory request operation, such as s store , or load, in order to enhance the adaptability of the system, therefore, all instructions in system should have included any memory request in the same system. And, for the reasons just given above, it would have been obvious to on e of ordinary skill in the art to make the load before a memory request as claimed .

5. As to the address generation for generating the addresses of the load requests and store request out of order, the patented claim 64 also taught execution of the plurality of instructions from the instruction window out of order (claim 64, col.25, lines

1-6), therefore, addresses of the load and store requests must have been generated in order to execute the instructions from the instruction window out of order.

6. Claim 68 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 26 of U.S. Patent No. 5, 659,782. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the current claim does not recite the load request was made before all instructions as specifically recited in the patent claim 26, one of ordinary skill in the art should be able to recognize the all instructions in the instruction window as recited in the patented claim 26 could be applicable for a load before any instructions including a memory request operation, such as a store, or load, in order to enhance the adaptability of the system, therefore, all instructions in system should have included any memory request in the same system, And, for the reasons just given above, it would have been obvious to on e of ordinary skill in the art to make the load before a memory request as claimed .

7. As to the "super scalar microprocessor" recited in the current claim 68, the patented claim 26 already recited "computer" (see preamble) used for executing "plurality of instructions" "out of order" (col.21, lines 23-30 , claim 26) , which would have been recognized by one of ordinary skill in the art that execution of plurality of instructions out of order was a characteristic feature of a super scale instructing processing.

8. Claim 93 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 49 of U.S. Patent No. 5,987,593. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the current claim does not recite the load request was made before all instructions as specifically recited in the patent claim 49, one of ordinary skill in the art should be able to recognize the all instructions in the instruction window as recited in the patented claim 49 could be applicable for a load before any instructions including a memory request operation, such as a store or load, in order to enhance the adaptability of the system, therefore, all instructions in system should have included any memory request in the same system. And, for the reasons just given above, it would have been obvious to on e of ordinary skill in the art to make the load before a memory request as claimed .

9. As to the super scalar microprocessor " recited in current claim 93, the patented claim 49 already recited "computer " (see preamble) used for executing "plurality of instructions" "out of order" (col.23, lines 45-46, claim 49) , which would have been recognized by one of ordinary skill in the art that execution of plurality of instructions out of order was a characteristic feature of a super scale instructing processing..

10. Claim 107 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 49 of U.S. Patent No. 5,987,593. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the current claim does not recite the load request was made before all instructions as specifically recited in the patent claim 49, one of

ordinary skill in the art should be able to recognize the all instructions in the instruction window as recited in the patented claim 49 could be applicable for a load before any instructions including a memory request operation, such as a store or load, in order to enhance the adaptability of the system, therefore, all instructions in system should have included any memory request in the same system. And, for the reasons just given above, it would have been obvious to on e of ordinary skill in the art to make the load before a memory request as claimed .

11. As to the address generation for generating the addresses of the load requests and store request out of order as recited in the current claim 107, lines 12-13, the patented claim 49 also taught execution of the plurality of instructions from the instruction window out of order (claim 49, col.23, lines 45-46), therefore, addresses of the load and store requests must have been generated in order to execute the instructions from the instruction window out of order.

12. Claim 123 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 19 of U.S. Patent No. 5,659,782. Although the conflicting claims are not identical, they are not patentably distinct from each other because although the current claim 123 does not specifically recited the RISC superscalar as recited in the patented claim 19, it would have been obvious to omit the RISC feature of the super scalar as the patented claim already taught that the RISC is a specific type of a superscalar, such as RISC superscalar (claim 19, line 1),

therefore, one of ordinary skill in the art should be able to recognize the use of a more general feature of the superscalar from the more specific superscalar , such as the RISC superscalar, as taught in patented claim 19 in order to achieve the general application of the superscalar, and for this reason , provided a motivation. Furthermore, "RISC" in a preamble does not add any substance into the completeness of the body of the claim. Therefore, no patentable weight is given unless a specific format of function(s) of the RISC to fulfill the completeness of the claim scope can be found.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 23-26,30-32, 33, 39 , 40, 41, 42, 46, 47, 52, 53, 57, 58,60,61, 67, 68-71, 76,77, 78, 79,83,84,85,86, 90,91,92, 93,99,100, 101,102,104,105,106, 107, 111, 112, 117-119, 120,121 , 122, 123, 124,125,126,127, 128,130-132,133-135 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popescu et al. (5,487,156) In view of Papworth (4,760,519) .

14. As to claims 23,26,33,40, 42, 47, 68-70, 78, 92, 93, 102, 106, 107, 112, 122, Popescu disclosed a microprocessor for executing instructions obtained an instruction store [cache] comprising at least :

a)fetch circuit [9] to fetch instructions from instruction store [cache], the instructions being in program order (e.g. see fig.2);

b) buffer [11] to buffer the instructions from the fetch circuit (fig.2);

c)execution unit for executing plurality of instructions our of in order (see the execution in col.6, lines 38-49, col.7, lines 3-49, col.8, lines 1-27, col.);

d)load store unit adapted to make load requests out of order before a memory request , wherein a second instruction [store] preceded the load instruction (e.g. see the parallel instructions for execution with the older instructions in col.8, lines 15-27, see also how the dependencies detection was done for the load in col.8, lines 28-67, col.9, lines 1-14, the load could be sent before the store with unmatched address);

e) load dependency detection for detecting address collision or write pending for a given load (e.g. see the unsafe state due to address match and the waiting for the memory access in col.8, lines 32-55);

e)register file comprising temporary registers (see col.9, lines 1-27);

f) address path configured to transfer data from memory to the execution unit ();

g) executing in one clock cycle (e.g. see the improved parallel execution in an instruction cycle in col.8, lines 15-27).

15. Popescu did not specifically teach the alignment of the data to permit the word boundary or to return on word boundary as claimed. However, Papworth disclosed a system including alignment of word boundary (see col.13, lines 18-30) . It would have been obvious to one of ordinary skill in the art to use Papworth in Popescu for including the alignment of the word boundary as claimed because the use of Papworth could provide Popescu the storage capability to adapt to specific word length, thereby increasing the adaptability of the instruction storage, and it could be readily achieved by predefining the alignment circuit of Papworth into Popescu with a predetermined set of the data format, such as the word length, and the boundary parameters, so that the correct alignment of the data word could be recognized by Popescu in order to enhance the adaptability of the processing system in Popescu, and for the above reasons, provided a motivation.

16. As to claims 24,25, Popescu also included address generation (e.g. see col.8, lines 29-35, see also lines 60-65 for store address calculation).

17. AS to claims 30, 31, Popescu also included dependencies detection of the load and store (e.g. see the detection of the older store with the current load in col.8, lines 29-68).

18. AS to claims 39,83, 84, 99, 100, 120,121, Popescu also included dependences detection store to load (e.g. see the unsafe state due to address match and the waiting for the memory access in col.8, lines 32-55).

19. As to claims 32, 41,46,85,101,111, Popescu also included relative age of the instructions (e.g. see col.4, lines 59-64).

20. As to claims 53,58, 61, 71, 86, Popescu also included store request in program order (e.g. see the store in col.8, lines 32-35, col.8, lines 3-6).

21. As claims 123,124, 130, 131, 132, Popescu also included at least :

a) calculation of the address and transferring the address to a load store unit (e.g. see col.8, lines 60-65)

b) determining the load and store instructions (e.g. se col.8, lines 29-65);

c) making request based on a priority scheme including a load [load] out of an ordering so the load can be made before a memory request [store] , wherein the load corresponding to a first instruction ,and the memory request including a second instruction (e.g. see . see the parallel instructions for execution with the older instructions in col.8, lines 15-27, see also how the dependencies detection was done for the load in col.8, lines 28-67, col.9, lines 1-14, the load could be sent before the store with unmatched address);

d) determining if load can be executed out of order, executing the load using generated address corresponding to a store preceding the load (see the unmatched address of the store and load in col.8, lines 29-67).

22. Popescu did not specifically show the alignment of he requested data as claimed. However, Papworth disclosed alignment of data requested (see col.13, lines 18-30). The reasons of the obviousness were already set forth in paragraph # 15 above, therefore, it will not be repeated herein.

23. As to claim 125, Popescu also included a temporally buffer (e.g. see col.7, lines 28-34).

24. As to claim 126, 127, Papworth also included bypass of a temporary buffer (e.g. see col.17, lines 28-39).

25. As to claims 52, 57, 60, 67, 76, 77, 90, 91, 104, 105, 117-119, 128, Papworth also included merge of the data from memory [77, 85] with the destination register [205,206] (see col.14, lines 48-68).

26. As to claim 133, Popescu also included the incorrectly modified system state (e.g. see the match bit and locker bits in col.7, lines 35-67).

27. AS to claim 134, Papworth also included merge of the data from memory [77, 85] with the destination register [205,206] (see col.14, lines 48-68).

28. AS to claim 135, Popescu also included a register file (e.g. see col.7, lines 28-52).

29. Claim 51, 56, 59 , 66, 75 ,89, 103, 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popescu in view of Papworth as applied to claims 23, 26, 33, 42, 68, 79, 93 , 107 above, and further in view of Jones et al. (4,794,517).

30. As to claims 51,56, 59 , 66, 75 ,89, 103, 116, since no specific features of the memory mapped I/O are being reflected in the claim, it is assumed the memory mapped I/O was directed to a general type of memory mapped I/O. Applicant is welcome to provide feedback in the next response. Neither Popescu nrorPapworth specifically showed the memory mapped I/O as claimed. However, Jones disclosed a memory mapped I/O (e.g. see col.6, lines 36-49). It would have been obvious to one of ordinary kill in the art to use Jones in Popescu for including the memory mapped I//O as claimed because the sue of Jones could provide Popescu the ability to adapt to specific request of a given peripheral device, thereby expanding the system's interface structure, and it could be done by configuring the memory I/O parameters of Jones, such as the corresponding address space of he I/O into Popescu so that the memory mapped I/O requests of Jones could be recognized by Popescu in order to enhancing the interface structure of the system, and therefore, provided a motivation.

31. Claims 27-29, 36, 37 ,38,43-45, 80-82, 96-98, 108-110 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art od record further teaches the alignment to generate plurality of memory requests in response to a single instruction when the operand of the single instruction falls on a word boundary.

32. Claim 34, 48, 54, 62, 72, 87, 94 , 113 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the address generation for the load and store requests as soon as all operands are valid and the address generation circuitry is available for address generation.

33. Claims 35, 50, 55, 65, 74, 88, 95, 115 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the generated address included linear and physical addresses, and the generation of the physical address corresponding o the linear address.

34. Claims 52, 57, 60, 67, 76, 77, 90, 91, 104, 105, 117-118 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the merge of the data returning from the memory with the initial contents of the destination register.

35. Claims 49, 65,66, 73, 114 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the linear address including the segment base, base register and scaled index register.

36. Claim 129 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the comparison of the load with the first and the last address for an older unretired store operation.

37. Clams 136-140 are allowable over the art of record for specifically reciting the combined features of the load out of order, the retiring the portion of the data provided from a cache according to the load address, the data having been aligned if the load address was unaligned if the load does not dependent from the store instruction, and retiring the portion of the load data according to the store data received

from the store instruction if the load instruction does not dependent from the store instruction,

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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